GIRLS' HIGH SCHOOL AND COLLEGE

2020-2021

CLASS 12 B

COMPUTER SCIENCE

WORKSHEET -04

CHAPTER- COMPUTER HARDWARE

Note: Parents please ensure that your ward refers to a computer science book/internet for two days to read the topic Computer Hardware.

Reference Book: Computer Science with Java for class 12 by Sumita Arora

Website: geeksforgeeks.org

Introduction:

- Gates are digital (two-state) circuits because the input and output signals are either low voltage (denotes 0) or high voltage (denotes 1).
- There are three basic gates: NOT, AND and OR
- There are four other gates: NOR, NAND, XOR and XNOR.
- The design and maintenance of digital computers are greatly facilitated by the use of Boolean algebra and logic circuits. Logic networks are designed making use of logic gates.
- Logic gates are used in following applications:
  - ADDER
    - -Half Adder
    - -Full Adder
  - ENCODER
  - DECODER
  - MULTIPLEXER

Answer the following questions:

1. Draw the two-input truth table and gate for all the three basic gates.
2. Design a circuit to realize the following:
   i. F(A,B,C) = AB + AC' + A'B'C
   ii. F(X, Y, Z) = (X + Y) . (X' + Z') . (Y + Z)

3. Draw the truth table for two input XOR gate and two input XNOR gate. What is the relation between the two? Write the SOP expression for XNOR.
4. Show that the dual of exclusive OR is equal to its complement.
5. Why NAND an NOR are called Universal gates?
6. Draw the truth table of 2-input NAND gate.
7. Draw all the three basic gates with NAND gate.
8. Draw all the three basic gates with NOR gates.
9. Draw the logic circuit of NOR using NAND gate only.
10. Draw the circuit diagram using NAND-to-NAND logic only for the following functions:
    i. F = AB'C + C'B
    ii. F = YZ + XZ
11. Draw the circuit diagram using NOR-to-NOR logic only for the following functions:
    i. F = A . (B' + C)
    ii. F = (X + Y) . (Y + Z) . (Z + X)
12. Draw the truth table and logic circuit diagram for Half Adder. Also write the SOP expression for sum and carry.
13. Draw the truth table and logic circuit diagram for Full Adder. Also write the SOP expression for sum and carry.
14. Differentiate between Half adder and Full adder.
15. What is an Encoder? Draw the logic circuit for Decimal-to-Binary Encoder.
16. Draw the Encoder circuit to convert A-F hexadecimal number to binary.
17. What is Decoder? Draw the truth table and logic circuit for 3X8 Decoder.
18. What is a Multiplexer? Write the applications of Multiplexer.
19. Draw the circuit diagram for a 8 : 1 multiplexer.
20. Given the Boolean function: $F(A,B,C,D)= \sum (2, 3, 4, 6, 7, 9, 11, 12, 13, 14, 15)$
    i. Reduce the above expression by using 4-variable K-Map, showing the various groups (i.e. octal, quads and pairs).
    ii. Draw the logic gate diagram of the reduced expression. Assume that the variables and their complements are available as inputs.
21. Given the Boolean function: $F(P,Q,R,S)= \prod (0, 1, 4, 5, 6, 7, 8, 9, 13, 15)$
    i. Reduce the above expression by using 4-variable K-Map, showing the various groups (i.e. octal, quads and pairs).

ii. Draw the logic gate diagram of the reduced expression. Assume that the variables and their complements are available as inputs.

22. An insurance company issues a policy to an applicant only when the applicant satisfies at least one of the following conditions:

- The applicant is a married male of age 25 years or above.
- The applicant is a female who never had a car accident.
- The applicant is married female and has had a car accident.
- The applicant is a male below 25 years.
- The applicant is not below 25 years and has never had a car accident.

The inputs are:

M: The applicant is married

S: The applicant is a male

C: The applicant has had a car accident

Y: The applicant is below 25 years

The output is: I- Denotes Policy Issued [1 indicates YES and 0 indicates NO in all cases]

i. Draw the truth table for the inputs and outputs given above and write the SOP expression for I(M, S, C, Y).

ii. Reduce I (M, S, C, Y) using Karnaugh's Map.

Draw the logic gate diagram for the reduced SOP expression for I (M, S, C, Y) using AND and OR gates. You may use gates with two or more inputs. Assume that the variable and their complements are available as inputs.

23. Reduce the following expression using the laws of Boolean algebra. Draw the logic gate diagram for the simplified expression:

F = A . (A' + B) . C . (A + C)

24. A provisional store announces a special discount on all its products as a festival offer only to those who satisfy any one of the following conditions:

- If he/she is an employee of the store and has a service of more than 10 years.

OR

- If he/she is a regular customer of the store whose age is less than 65 years and is not an employee of the store.

OR

- If he/she is a senior citizen but not a regular customer of the store.

The inputs are:

E: Employee of the store

R: Regular customer of the store

S: Service of the employee is more than 10 years

C: Senior citizen of 65 years or above

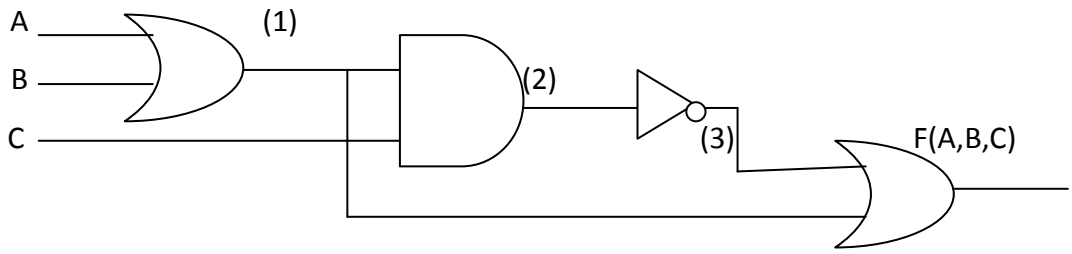
The output is: X- Denotes eligible for discount [1 indicates YES and 0 indicates NO in all cases]

i. Draw the truth table for the inputs and outputs given above and write the SOP expression for X (E, R, S, C).

ii. Reduce X (E, R, S, C) using Karnaugh's Map.

Draw the logic gate diagram for the reduced SOP expression for X(E, R, S, C) using AND and OR gates. You may use gates with two or more inputs. Assume that the variable and their complements are available as inputs.

25. From the logic circuit diagram given below, name the parts (1), (2), (3) and finally derive the Boolean expression and simplify it.



----------END----------